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Democratizing Silicon:

The Open Source paradigm of chip design

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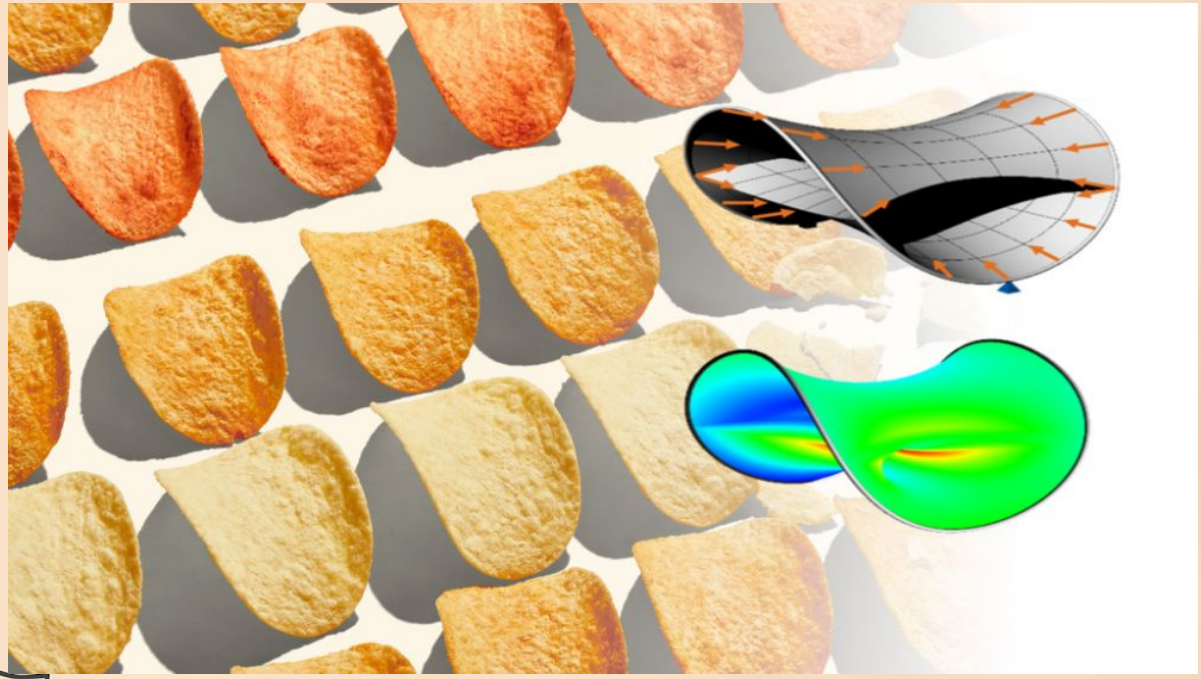

Source: MechHead (Food Science – Geometry of Pringles)

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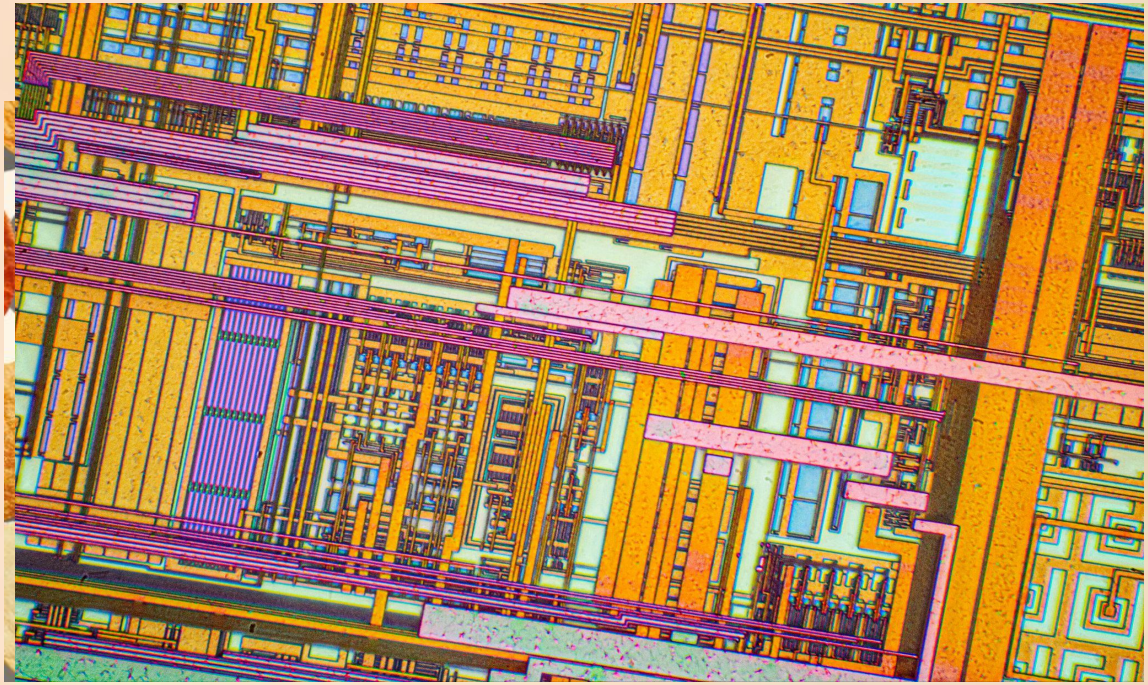

Source: Wikipedia

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Why Open-Source Chip design?

- Country A, a powerful nation, controls all advanced chips, tools, and fabs.
- Small, developing Country B relies on these for healthcare, defense, and industry.
- A political embargo, possibly triggered by something minor, could sever B's access to vital silicon.
- Open-source chip design offers Country B self-reliance, resilience, and permissionless innovation.

And Now a Twist…

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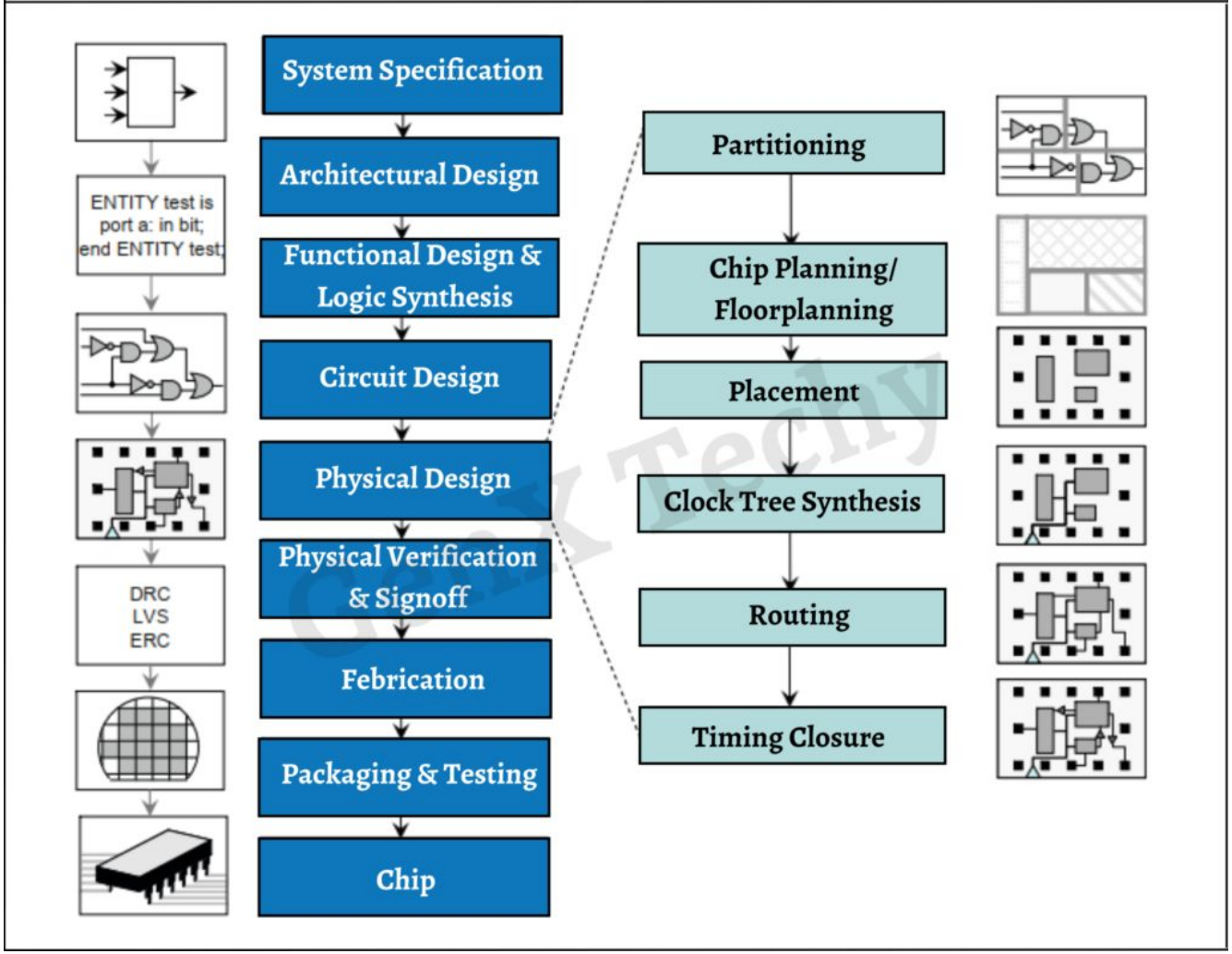

Source: GenXTechy (VLSI Design Flow Guide)

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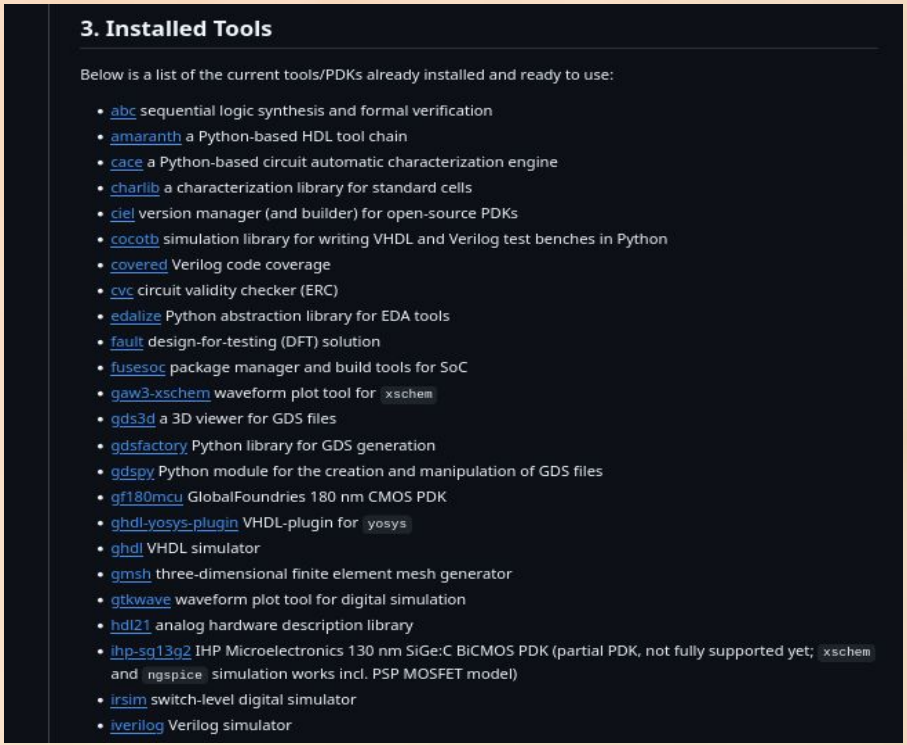
Enabling Open-Source Silicon



3. Installed Tools

Below is a list of the current tools/PDKs already installed and ready to use:

- abc sequential logic synthesis and formal verification
- amaranth a Python-based HDL tool chain
- cace a Python-based circuit automatic characterization engine
- charlib a characterization library for standard cells
- ciel version manager (and builder) for open-source PDKs
- cocotb simulation library for writing VHDL and Verilog test benches in Python
- covered Verilog code coverage
- cvc circuit validity checker (ERC)
- edalize Python abstraction library for EDA tools
- fault design-for-testing (DFT) solution
- fusesoc package manager and build tools for SoC
- gaw3-xschem waveform plot tool for `xschem`
- gds3d a 3D viewer for GDS files
- gdsfactory Python library for GDS generation
- gdspy Python module for the creation and manipulation of GDS files
- gf180mcu GlobalFoundries 180 nm CMOS PDK
- ghdl-yosys-plugin VHDL-plugin for `yosys`
- ghdl VHDL simulator
- gmsh three-dimensional finite element mesh generator
- gtkwave waveform plot tool for digital simulation
- hdl21 analog hardware description library
- ihp-sg13g2 IHP Microelectronics 130 nm SiGe:C BiCMOS PDK (partial PDK, not fully supported yet; `xschem` and `ngspice` simulation works incl. PSP MOSFET model)
- irsim switch-level digital simulator
- iverilog Verilog simulator

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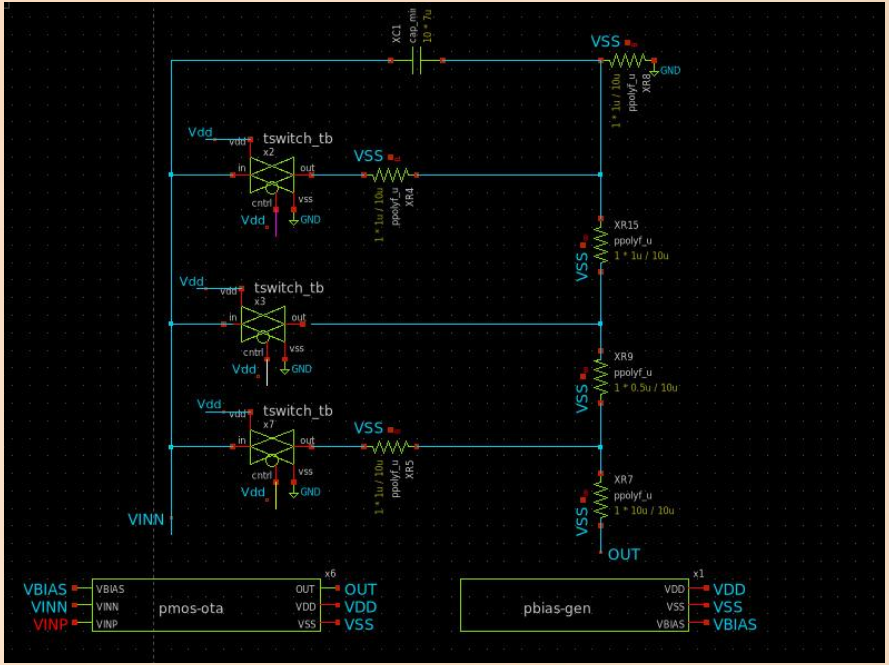
My Tapeout experience



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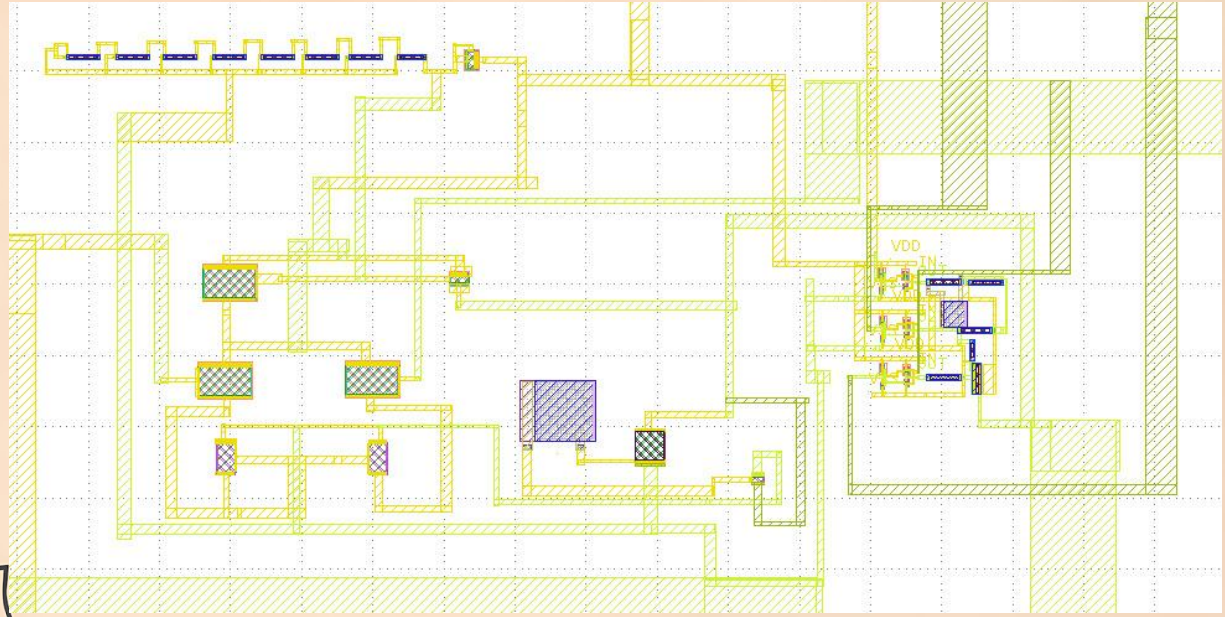

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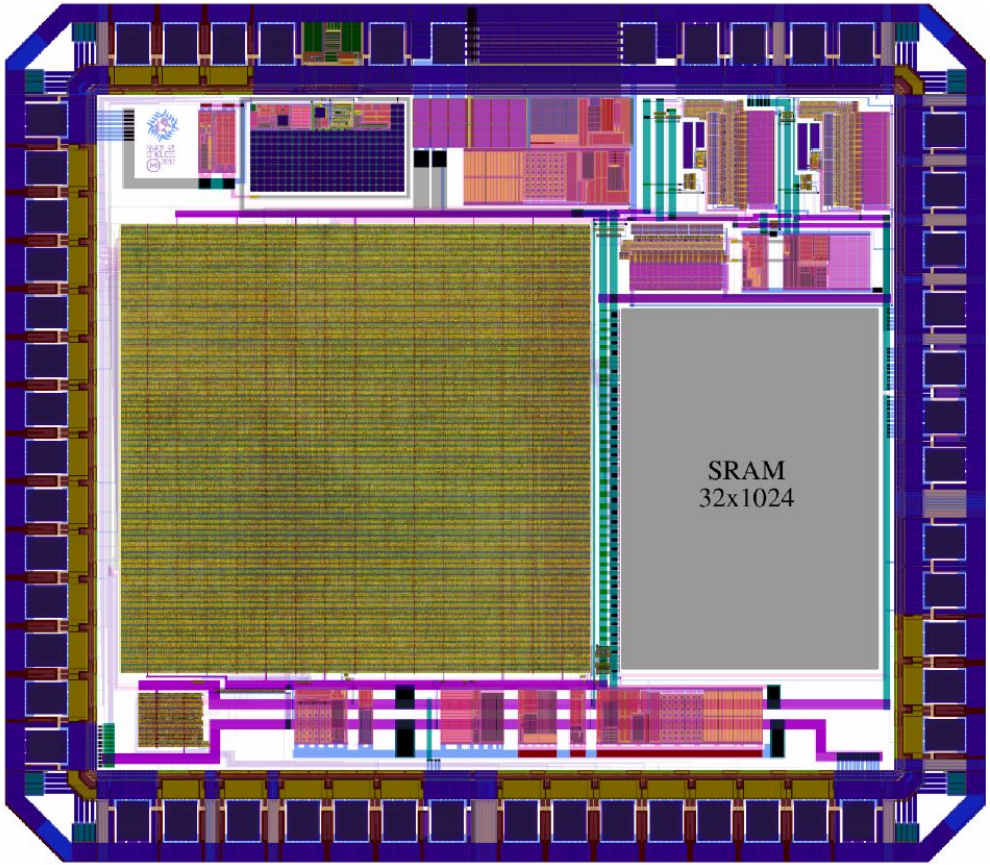
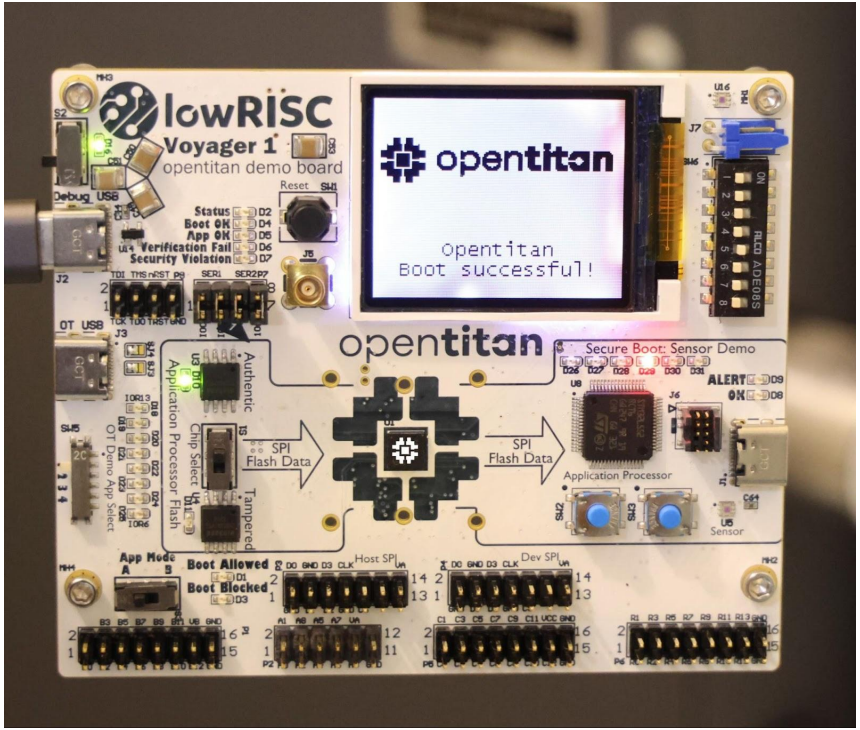
Open-Source Silicon Successes

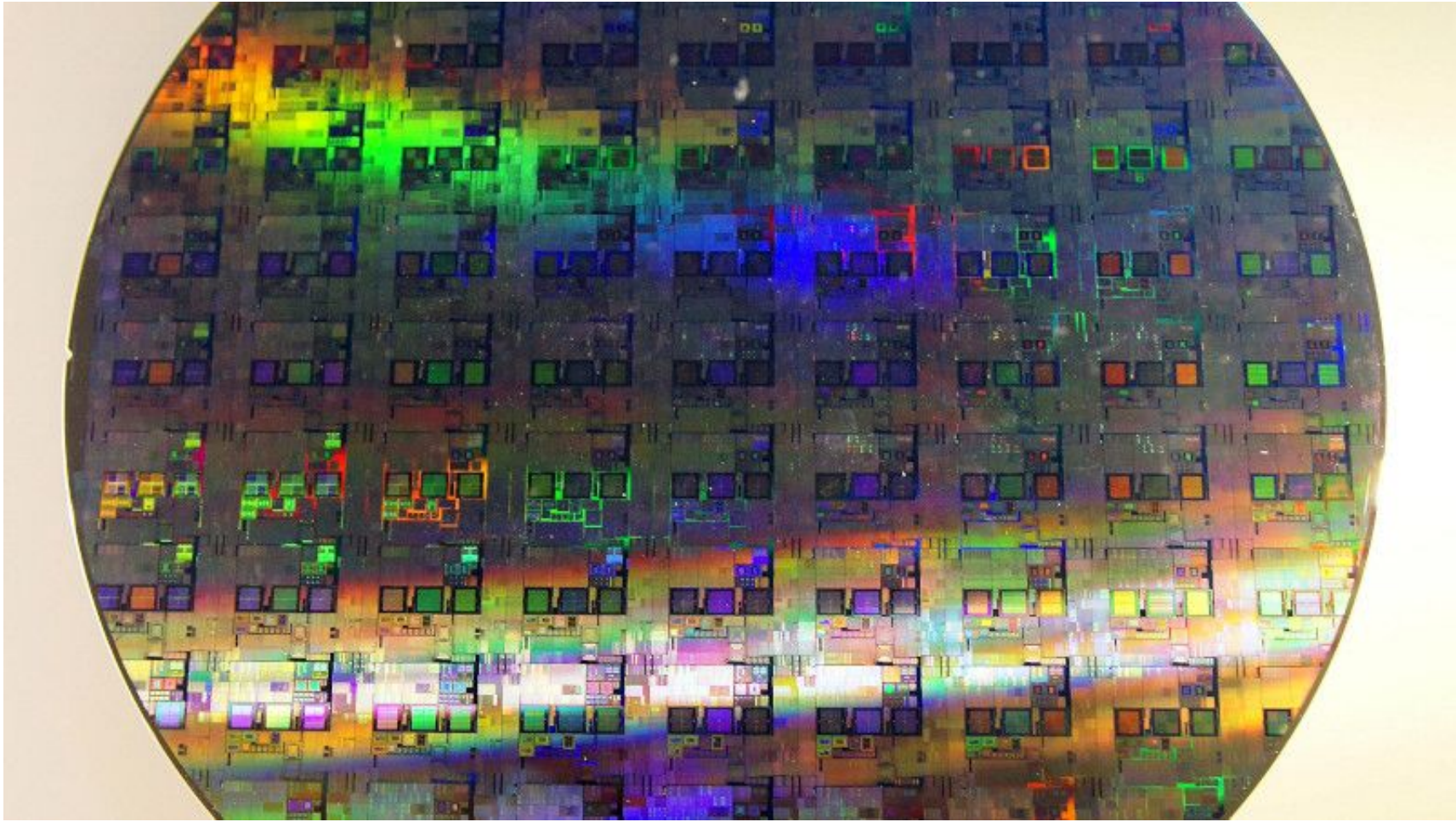
- OpenTitan provides a critical open-source root of trust
- PicoRV32 and Ibex are successful minimal embedded cores
- BOOM core demonstrates high-performance out-of-order design
- Open silicon enables security, education, research, and startups



Source: Hackster.io (Raven RISC-V Microcontroller Project)



Source: Google Open Source Blog (OpenTitan Production Silicon Update)



Source: Hackaday (SkyWater 130nm Open-Source ASIC News)

What can we do?

- Join the growing open hardware design communities now
- Start experimenting with open-source tools today
- Run your very first Verilog simulation successfully

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My Tapeout: PGA

GF180 Tutorial by Efabless

JKU IIC-OSIC-TOOLS

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Thank You!

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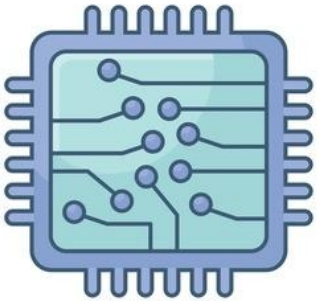

- dig in remote places
- extract extremely rare rocks
- perform a forming spell on the rocks
- extreme heat and pressure are required
- inscribe microscopic arcane sigils into your magical stones
- imbue the stones with lightning
- the stones gain anima
- the stones speak in a language incomprehensible to all mankind
- certain trained warlocks can control the powers of the stones
- they learn the language of the stones
- the warlocks harness the magical stones powers to bring forth light and image
- the rest of the population is in awe
- you can now access cat memes anywhere you want from a palm of your hand

Source: Reddit

Any Questions?